Docket No. 1999-1337.01/US

Application For Letters Patent

for

REDUCED ASPECT RATIO DIGIT LINE CONTACT PROCESS FLOW USED DURING THE FORMATION OF A SEMICONDUCTOR DEVICE

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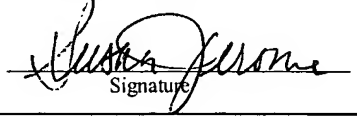

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REDUCED ASPECT RATIO DIGIT LINE CONTACT PROCESS FLOW USED DURING THE FORMATION OF A SEMICONDUCTOR DEVICE

[0001] This is a division of US Serial No. 09/765,885 filed January 16, 2001 and issued March 23, 2004 as US Patent No. 6,709,945.

Field of the Invention

[0002] This invention relates to the field of semiconductor processing, and more particularly to a method for forming a contact and a container capacitor for a semiconductor device such as a dynamic random access memory.

Background of the Invention

[0003] During the manufacture of a semiconductor device such as dynamic random access memories (DRAMs), static random access memories (SRAMs), microprocessors, and logic devices, several structures are commonly formed. For example, contact openings to a conductive layer such as doped monocrystalline silicon wafer, a polycrystalline silicon (polysilicon) layer, or a metal feature through a dielectric layer such as tetraethyl orthosilicate (TEOS) and/or borophosphosilicate glass (BPSG) can be formed. Further, openings are commonly formed within a dielectric layer as an early step in the formation of a container capacitor in a memory device.

[0004] FIGS. 1-6 depict a conventional process used during the formation of a semiconductor memory device such as a DRAM to form storage capacitors and digit line contacts. FIG. 1 depicts a semiconductor wafer substrate assembly comprising a semiconductor wafer 10, field oxide 12, doped wafer areas 13, transistor control gates typically comprising a polysilicon gate 14A and silicide 14B, and surrounding dielectric typically comprising gate oxide 16A, nitride spacers 16B, and capping layer 16C, for example TEOS. FIG. 1 further depicts polysilicon contact pads including pads 18 to which container capacitors will be electrically coupled and pads

20 which will form a portion of a digit line contact to the wafer 10. The pads are separated by a dielectric layer 22, for example BPSG. Also depicted is a second layer of dielectric 24 which can be one or more layers of TEOS and/or BPSG. A layer of photoresist 26 defines openings 28 which overlie pads 18 to which the container capacitors will be electrically coupled. The structure of FIG. 1 is exposed to a vertical anisotropic etch which removes the dielectric layer 24 selective to the polysilicon contact pads 18.

[0005] FIG. 2 depicts openings 30 which result from the etch of the FIG. 1 structure. The etch exposes pads 18, which in turn contact doped regions 13. Pads 18, therefore, decrease the amount of oxide which the etch of the FIG. 1 structure must remove. Without pads 18, the etch would be required to remove the additional thickness of oxide layer 22 to expose doped regions 13.

[0006] After forming the openings, a blanket layer of hemispherical silicon grain (HSG) 32 is formed over exposed surfaces including pads 18. Subsequently, the openings are filled with a sacrificial protective material such as photoresist (not depicted) and the HSG and a portion of dielectric 24 are etched, for example using chemical mechanical polishing (CMP). This removes the HSG from the horizontal surface of dielectric 24. Any protective material remaining within opening 30 is removed.

[0007] Next, blanket layers of cell nitride 34 and top plate polysilicon 36 are formed over the surface of the assembly as depicted in FIG. 3. A patterned photoresist layer 38 is provided which defines the storage nodes and capacitor top plate. After the etch, the photoresist 38 is removed.

[0008] As depicted in FIG. 4 another dielectric layer 40 such as BPSG is deposited and planarized and a patterned photoresist 42 is formed over dielectric 40. Opening 44 within the photoresist layer overlies the digit line contact pad 20. A vertical anisotropic etch is performed which etches through dielectric layers 40 and 24 to provide a contact opening 50 and to

expose the digit line contact pad 20 as depicted in FIG. 5. The etch exposes pad 20, which in turn contacts doped region 13. Pad 20, therefore, decreases the amount of oxide which the etch of the FIG. 4 structure must remove. Without pad 22, the etch would be required to remove the additional thickness of oxide layer 22 to expose doped region 13. Finally, as depicted in FIG. 6, a conductive plug 60 typically comprising tungsten is formed within opening 50 and a metal digit line runner 62, typically aluminum, is formed over dielectric layer 40 to electrically contact the plug 60 to provide a digit line.

[0009] One problem with a process such as that described above is that the etch of the digit line contact opening 50 to expose the digit line contact pad 20 requires etching through a very thick series of dielectric layers. With current processes the ratio of the contact opening height to the width (i.e. the "aspect ratio") can be 10:1 or greater. For example, layer 24 depicted in FIG. 4 can have a thickness of 14,000 angstroms (Å) or more, and layer 40 can have a thickness of 4,000Å for a total of 18,000Å of dielectric to etch through to form a contact about 1,150Å wide for an aspect ratio of about 15:1. As the aspect ratio of openings increases the opening becomes increasingly difficult to form reliably. Contact locations in a periphery of a semiconductor device (see 174 in FIG. 17, for example) often do not have pads 18, 20 which further increases the aspect ratio. Problems forming high aspect ratio contacts include difficulty in etching the bottom portion of the dielectric layer, in maintaining the proper diameter of toward the top of the opening, and in filling the contact opening with conductive material subsequent to its formation.

[0010] A method for forming a contact opening which reduces or eliminates the problems described above would be desirable.

Summary of the Invention

[0011] The present invention provides a new method that reduces problems associated with the manufacture of semiconductor devices, particularly

problems resulting from contact etches and fills requiring a high aspect ratio. In accordance with one embodiment of the invention a portion of a digit line contact opening is etched to expose a digit line contact pad, then the opening is filled with conductive material to form a digit line contact plug to the pad. A storage capacitor is subsequently formed and the remainder of the digit line plug and digit line runner are formed. This process decreases the aspect ratio of the contact openings which must be formed, and may provide increased capacitance of the storage capacitor by allowing an increased height of the capacitor as will be described in detail below.

[0012] Other advantages will become apparent to those skilled in the art from the following detailed description read in conjunction with the appended claims and the drawings attached hereto.

Brief Description of the Drawings

[0013] FIG. 1 is a cross section depicting an opening in a photoresist layer to define container capacitors within a dielectric layer;

[0014] FIG. 2 depicts the FIG. 1 structure after etching the dielectric layer and forming a blanket hemispherical silicon grain (HSG) layer;

[0015] FIG. 3 is a cross section of the FIG. 2 structure subsequent to a planarization step and after forming a cell dielectric layer, a cell top plate layer, and a patterned photoresist layer to define a storage capacitor;

[0016] FIG. 4 is a cross section of the FIG. 3 structure after etching the cell dielectric and top plate, after formation of a planarized dielectric layer and formation of a patterned photoresist layer to define digit line contacts;

[0017] FIG. 5 is a cross section of the FIG. 4 structure after etching the digit line contact opening;

[0018] FIG. 6 is a cross section of the FIG. 5 structure after forming a contact plug and a metal runner to form a digit line;

[0019] FIG. 7 is a cross section of a first embodiment of the invention having a patterned photoresist layer which defines a digit line contact opening in a dielectric layer;

[0020] FIG. 8 is a cross section of the FIG. 7 structure subsequent to etching the dielectric layer and forming a blanket conductive plug layer within the opening;

[0021] FIG. 9 is a cross section of the FIG. 8 structure after planarizing the blanket plug layer to form a first portion of a digit line contact plug and after forming a blanket dielectric layer over the first conductive plug portion and a patterned photoresist layer which defines the container capacitor in a dielectric layer;

[0022] FIG. 10 depicts the structure of FIG. 9 subsequent to etching the dielectric layer to define the container capacitor, and subsequent to forming a blanket HSG layer and a protective photoresist layer within recesses defined by the HSG;

[0023] FIG. 11 depicts the FIG. 10 structure after a planarization step, after removing the photoresist layer, and after forming a cell dielectric layer, a capacitor top plate layer, a dielectric layer, and a patterned photoresist layer which defines openings to the digit line contact plug previously formed;

[0024] FIG. 12 depicts the structure of FIG. 11 subsequent to an etch which exposes the digit line contact plug;

[0025] FIG. 13 depicts the structure of FIG. 12 subsequent to forming a spacer dielectric layer;

[0026] FIG. 14 depicts the FIG. 13 structure after an anisotropic etch of the spacer layer and the formation of a digit line runner layer which also forms a portion of the digit line contact plug;

[0027] FIG. 15 depicts a cross section for a second embodiment of the invention similar to that of FIG. 9 having a digit line contact opening aspect ratio similar to that of conventional devices;

[0028] FIG. 16 depicts a cross section of the FIG. 15 structure after completion of various steps of the inventive embodiment; and

[0029] FIG. 17 is a cross section depicting various additional exemplary structures which can be formed during the process of FIGS. 9-16.

[0030] It should be emphasized that the drawings herein may not be to exact scale and are schematic representations. The drawings are not intended to portray the specific parameters, materials, particular uses, or the structural details of the invention, which can be determined by one of skill in the art by examination of the information herein.

Detailed Description of the Preferred Embodiment

A first embodiment of an inventive method used during the formation of a semiconductor device is depicted in FIGS. 7-14. FIG. 7 depicts a semiconductor substrate assembly comprising a semiconductor substrate such as a wafer 10, field oxide 12, a transistor control gate comprising a polysilicon gate 14A and silicide 14B, surrounding dielectric including gate oxide 16A, nitride spacers 16B, and capping dielectric 16C, for example comprising tetraethyl orthosilicate (TEOS) and nitride. FIG. 7 further depicts capacitor storage node contact pads 18 comprising polysilicon, a digit line contact pad 20 comprising polysilicon, and an overlying dielectric 24 such as borophosphosilicate glass (BPSG) which has been chemically-mechanically

planarized (CMP) to about 14,000Å thick in this exemplary embodiment in accordance with the conventional device described above. A patterned photoresist layer 70 defines an opening 72 to the digit line contact pad 20. The structure depicted in FIG. 7 can be manufactured by one of ordinary skill in the art from the description herein.

[0031] After forming the FIG. 7 structure, BPSG layer 24 is etched to expose the digit line contact pad 20. An etch comprising an atmosphere of CHF_3 at a flow rate of 50 standard cubic centimeters (sccm), a temperature of about 50°C, and a pressure of about 15 millitorr (mT) would remove about 40Å of oxide/minute. Thus for a BPSG layer 24 between about 14,000Å as described above, a duration of about 5.8 minutes would be sufficient. The contact opening at the bottom, in accordance with the conventional embodiment described above, should have a minimum width at the bottom of 1,150Å.

[0032] Subsequently, a blanket metal layer 80, for example tungsten, is formed within the opening in BPSG 24 and overlying the BPSG layer as depicted in FIG. 8. A tungsten layer having a thickness of at least half as thick as the maximum width of opening 72 which defines the opening in the BPSG 24 can be formed using tungsten hexafluoride, WF_6, and silane, SiH_4, to begin the tungsten deposition. The silane provides a silicon source to tie up free fluorine atoms which can damage the substrate. After the initial layer of tungsten is produced, the deposition process is enhanced by replacing the silane with hydrogen gas.

[0033] Next, the structure of FIG. 8 is planarized, for example using chemical mechanical polishing (CMP) with an ammonia-based slurry, to remove the metal overlying dielectric 24 and leaving a metal plug 90 within dielectric 24 as depicted in FIG. 9.

[0034] Another blanket dielectric layer 92 such as a TEOS layer between about 150Å and about 250Å, preferably about 200Å, is deposited over the plug 90 and the BPSG layer 24. TEOS can be formed using a liquid source such as $Si(OC_2H_5)_4$ introduced into a low pressure chemical vapor deposition (LPCVD) furnace between about 690°C and about 720°C. Other materials may also function for dielectric layer 92 such as a nitride, an oxynitride, or other similar diffusion barriers which are sufficient to prevent lower metal layers such as silicide gate portions 14B from oxidizing.

[0035] A patterned photoresist layer 94 is formed over the TEOS layer 92 to define openings 96 to container capacitor contact pads 18. An anisotropic oxide etch is performed on the structure of FIG. 9 to etch TEOS 92 and BPSG 24 to expose container capacitor contact pads 18 and to define the container capacitor. The oxide etch described previously relative to BPSG would sufficiently remove the TEOS and BPSG layers. The photoresist is removed.

[0036] Subsequently, a capacitor storage node layer 100 is formed over exposed surfaces as depicted in FIG. 10 and makes electrical contact with container capacitor contact pads 18. The storage node layer can be formed using any number of workable processes. For example, a texturized polysilicon layer having a nominal thickness of between about 300Å and about 1,500Å can be formed using an *in situ* polysilicon in an LPCVD furnace at about 535°C using silane and phosphine (PH_3) as source gasses. The wafer is moved to an oxidation furnace to receive a phosphorous deposition to a conductivity of between about 1E18 atoms/cm^3 to about 5E21 atoms/cm^3. A native oxide will form on the polysilicon surface. The wafer is subjected to a 60 second 100:1 hydrofluoric acid bath, which results in partial removal of the native oxide such that thin patches of oxide remain. Next, hemispherical silicon grain (HSG) is formed over the *in situ* polysilicon layer in an LPCVD furnace at 555°C using silane gas. The small oxide patches on the *in situ* surface give the polysilicon layer a rough surface. A target polysilicon thickness of between about 500Å and about 3,000Å would be sufficient depending on the width of the opening, and other thicknesses may be sufficient. Contact pads 18 are electrically coupled by physical contact with storage node 100 layer and with doped regions 13.

[0037] After forming HSG layer 100, the recess defined by the layer is filled with a sacrificial layer 102 such as photoresist. The surface of the FIG. 10 structure is then planarized, for example using CMP, to remove the HSG from the horizontal surface of the dielectric 92. The HSG within the opening remains to form the container capacitor storage plate. The thickness of material removed from the structure should be small enough so that a portion of dielectric layer 92, for example at least about 100Å remains subsequent to planarization. After this planarization step, the photoresist layer 102 is removed.

[0038] Next, a cell dielectric layer 110 such as cell nitride and a top plate layer 112 such as polysilicon are formed over the exposed surfaces. A cell nitride layer between about 85Å and 105Å can be deposited by processing the wafer in an LPCVD furnace using dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) gasses. A 2,000Å polysilicon top plate layer can be formed in an LPCVD furnace at about 620°C using an atmosphere of silane gas (SiH_4), or by using another workable method. As the polysilicon forms at a rate of about 4,000Å/hr, the process is performed for about 30 minutes to form the 2,000Å polysilicon layer as described above.

[0039] A dielectric layer 114, for example BPSG between about 4,000Å thick is formed and planarized. BPSG can be formed by employing an atmospheric pressure chemical vapor deposition (APCVD) system and silane, oxygen, phosphine (PH_3) and diborine (B_2H_6), and can be planarized using a reflow in a nitrogen purged atmospheric furnace at about 907°C for about 25 minutes followed by a three hour anneal at about 800°C. The dielectric 114, in this exemplary embodiment 4,000Å, is then patterned using a photoresist layer 116 formed over the BPSG layer 114 which defines an opening to the underlying digit line contact plug 90. The structure of FIG. 11 is etched using a vertical anisotropic etch, such as that described previously relative to BPSG adjusted for the present layer, which also etches the 2,000Å of polysilicon 112, the 95Å of cell nitride 110 and the 200Å of dielectric 92 to expose the plug 90 as depicted in FIG. 12.

[0040] After exposing the digit line plug 90, a polysilicon etch is performed to recess the exposed polysilicon 112 between nitride 110 and BPSG layer 114 as depicted in FIG. 13. To adequately recess a polysilicon layer 525Å thick, an etch comprising Cl_2 at a flow rate of about 7 sccm, SF_6 at a flow rate of about 25 sccm, He at a flow rate of about 35 sccm, O_2 at a flow rate of about 12 sccm, at a pressure of about 600 mTorr for about 18 seconds. After recessing the polysilicon 112, a dielectric layer is formed over the ends of polysilicon 112 which are exposed at the opening to the digit line plug 90. This can be accomplished by forming a dielectric layer 130 such as a conformal layer of nitride, or a planar layer such as TEOS, over exposed surfaces then performing a vertical spacer etch to result in the spacers 140 of FIG. 14. Alternately, a facet etch of the BPSG 114, for example using cations from an argon plasma to chip off protruding BPSG from the top corners of layer 114 and to redistribute or redeposit it to the sidewalls and to isolate polysilicon 112, would be sufficient and would eliminate the need for forming a separate dielectric layer. Such a process may be sufficient for any oxide or glass film with some modification, for example to adjust for various dopants which may affect the etch. It will be appreciated by one of ordinary skill in the art that this self-aligned isolation of the cell polysilicon reduces the possibility of shorting between the digit line plug and the cell polysilicon over conventional processes.

[0041] After forming the dielectric layer 140 over the exposed ends of polysilicon layer 112, a patterned metal layer 142 such as titanium and aluminum/copper is formed to contact the digit line plug 90 as depicted in FIG. 14. In one exemplary metal deposition process, argon gas is changed into a plasma and the ions are used to bombard titanium and aluminum/copper targets. Atoms of metal material are sputtered from the metal target to the wafer surface to form layer 142.

[0042] The inventive process disclosed above has the advantage over conventional processes that an excessive dielectric thickness does not need to be etched to form the digit line plug and the aspect ratio of the contact plug opening is reduced. The plug opening is, in effect, etched using two

separate etches. In the embodiment of the invention described above the two etches which define the plug are separated in time by an etch which defines the capacitor storage plate. Using the conventional process described herein in the Background of the Invention above, 18,000Å of dielectric was etched through using a single etch to form the plug opening. With the instant process, 14,000Å of oxide dielectric were removed from a first BPSG layer in a first etch. In a second etch, 4,000Å of dielectric, 2,000Å of polysilicon, 95Å of cell nitride, and 200Å of TEOS were removed to form a structure analogous to the plug of conventional processes. As the opening in each case is about 1,150Å, the aspect ratio of the first oxide etch is about 12:1, and in the second etch the aspect ratio is about 5.5:1.

[0043] In a second embodiment of the invention the aspect ratio of the conventional process is maintained for the etch of the FIG. 7 structure by forming a thicker layer 24, then the process is continued according to the first embodiment. With this second embodiment, a storage capacitor having a greater height and therefore a greater capacitance is formed. FIG. 15 depicts a structure similar to FIG. 9, except that the opening which forms plug 150 has the aspect ratio of the opening 50 of the conventional structure of FIG. 5. In this embodiment, dielectric layer 152 of FIG. 15 is about the same thickness as layers 24 and 40 (FIG. 5) combined. After forming the structure of FIG. 15, wafer processing continues as described above for the first inventive embodiment, adjusted for thicker layer 152, to result in the structure of FIG. 16. In comparing FIGS. 16 and FIG. 14, the storage capacitor comprises a greater height and surface area, and therefore an increased capacitance, with no increase in horizontal spacing. Thus this embodiment has the advantage over the conventional process of FIGS. 1-6 that a larger storage capacitor is formed without increasing the aspect ratio of the digit line contact plug.

[0044] In a third embodiment of the invention, the digit line contact plug opening has an intermediate aspect ratio between that of the first and second inventive embodiments. This third embodiment reduces the digit line contact opening aspect ratio, and therefore the difficulty of the etch,

but allows for a larger storage capacitor having a larger capacitance than is possible with conventional devices having a larger digit line contact opening aspect ratio.

[0045] It will be appreciated by one of ordinary skill in the art that various other features, such as silicide to improve polysilicon conductivity and various steps such as inspection and cleaning will be present depending on the design of the device which have been omitted from the FIGS. and description for simplicity of explanation.

[0046] In another embodiment layer 92 may not be required. Layer 92 protects underlying layers during high-temperature processing of the wafer subsequent to its formation. For example, the formation of layer 142 may require a high-temperature anneal depending on the material used. High-temperature steps such as the anneal can result in oxidation of various substructures such as silicide 14B, some of which have contacts formed thereto, depicted as layer 170 in FIG. 17. If the silicide oxidizes, the electrical properties of the contact can be degraded, and layer 92 reduces or eliminates oxidation of underlying layers. If high-temperature steps are not required, it may be possible to eliminate layer 92. However, layer 92 requires no additional masking steps. FIG. 17 further depicts a contact plug 172 to a doped region 174 in the wafer 10 formed simultaneously with the other contact plugs 90, 170.

[0047] A semiconductor device formed in accordance with the invention may be attached along with other devices to a printed circuit board, for example to a computer motherboard or as a part of a memory module used in a personal computer, a minicomputer, or a mainframe. The inventive device can be useful in electronic devices related to telecommunications, the automobile industry, semiconductor test and manufacturing equipment, consumer electronics, or virtually any piece of consumer or industrial electronic equipment.

[0048] While this invention has been described with reference to illustrative embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as additional embodiments of the invention, will be apparent to persons skilled in the art upon reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.